Saipranav Venkatakrishnan

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Education

University of Illinois Urbana-Champaign GPA: 3.84
B.S. in Computer Engineering August 2022–May 2026
John P. Desmond Electrical and Computer Engineering Scholarship Award Recipient

Related Coursework: Computer Organization and Design (ECE 411), Logic Synthesis (ECE 462), Data Structures and Algorithms (CS 225), Operating Systems Development (ECE 391), Digital Systems Lab (ECE 385), Applied Parallel Programming (ECE 408), Introduction to Algorithms and Models of Computations (CS 374), Photonic Devices (ECE 304), Quantum Systems (ECE 305), Quantum Information Theory (ECE 404)

Technical Skills

Programming Languages and Skills: SystemVerilog, C, C++, CUDA C++, Python, Lua, ASIC Design, Computer Vision, Object-Oriented Programming, Parallel and Multithreaded Programming, Networking, SIS, ABC

Libraries & Tools: Synopsys Design Compiler, Synopsys VCS, Verdi, Verilator, Vivado, Vitis, FPGA, Nvidia Nsight Compute, Nvidia Nsight Systems, Oscilloscope, Git, Arduino, Google Cloud, Docker, Kubernetes, Pytorch, Vulkan, Qiskit

Experience

ASIC Design Intern May 2026 – August 2026
NVIDIA Santa Clara, CA

Undergraduate Hardware Research Assistant December 2024 – Present
PlatformX Champaign, IL

- Designed an **architectural simulator** to profile AI Wafer-scale chip designs, helping find improvements to **bandwidth utilization** and **compute efficiency** through **heterogeneous core** designs
- Extended **GPGPU-Sim** (**cycle-accurate simulator**) with **C++** and automation scripts to enable detailed profiling of **memory access patterns** and **interconnect bandwidth**
- Applied simulator extensions to investigate architectural tradeoffs across various **high-speed interconnect** designs within **GPU Processing Clusters (GPCs)**, focusing on interactions between **L1 cache slices** and **streaming multiprocessors (SMs)** optimized for **AI workloads**

Computer Architecture (ECE 411) Course Staff August 2025 – Present
UIUC Computer Organization and Design Champaign, IL

- Trained students in designing and implementing **out-of-order RISC-V processors** with advanced features such as **non-blocking pipeline caching**, **branch prediction** and **recovery**, out-of-order **load/store units**, and **superscalar** execution
- Mentored students on **RTL debugging** across **pipeline** and **cache** projects, providing targeted design and verification support
- Orchestrated competition with fellow course staff to profile and test **30+ RISC-V processors**, ranking them on metrics related to **Power, Performance, and Area (PPA)**

Graphics Engineering Intern May 2025 – August 2025
Aechelon Technology Roeland Park, KS

- Integrating SMPTE ST 2110-compliant **UDP transmission** into the pC-Nova platform via NVIDIA Rivermax SDK, utilizing **GPUDirect and RDMA** with full kernel bypass to eliminate **CPU bottlenecks**
- Implemented 5 **GPU kernels** and custom **fragment shaders** to transform output media into various color (e.g., YUV, sRGB) and vector spaces for compatibility with heterogeneous display systems

Software Development Intern May 2024–November 2024
CME Group Chicago, IL

- Lead a team of 4 interns in developing an application to **monitor project deployments** to on-premises and cloud server for any **abnormal resource allocations** and stalls
- Won **first place** in an internal **CME Hackathon** to develop a **low-latency trading algorithm**, earning $1000 as the prize

Software Development Intern March 2023–August 2023
CME Group Champaign, IL

- Supervised a team of 5 intern through **creating** an internal **C++ library** to validate research papers about methods to foretell stock prices through corresponding future market data
- Configured a CME security compliant remote development environment and integrated over **3000+ lines** into the CME codebase

Projects

RV-32IM RISC-V Processor January 2025 – May 2025
Computer Architecture Project SystemVerilog, C++

- Designed and verified a pipelined, out-of-order, **N-way superscalar processor** based on the **RV32IM ISA**, with explicit register renaming
- Implemented a split Load/Store Unit for **speculative memory operations**, branch predictors, and **non-blocking pipelined cache**, including **functional coverage** metrics to assess verification completeness
- Performed synthesis and power-performance-timing (**PPA**) analysis using **Synopsys Design Compiler**; evaluated across multiple testcases for critical path delays, area constraints, and **dynamic power** efficiency
- Debugged RTL with waveform tracing using **Verilator** and **Verdi**; verification involved writing unit-level **SystemVerilog testbenches** and assertions to validate pipeline stages, and simulations were performed with industry tools (VCS-compatible)

Graphics Engine May 2024 – August 2024
Graphics Project C++, Vulkan

- Building a **graphics pipeline** from scratch using the **Vulkan SDK**, with over **6K lines of C++ code** written across the entire codebase for low-latency rendering
- Implemented 5+ core **graphics pipeline stages**, including input assembly, rasterization, fragment shading, and framebuffer presentation
- Developed a system to automate Vulkan pipeline creation and manage 5+ **shader modules** across multiple **render passes**

Spiking Neural Network October 2024 – January 2025
Hardware Synthesis and Neuromorphic Computing SystemVerilog, FPGA

- Researched **neuromorphic architectures** and deployed a **spiking neural network** on an FPGA trained on the **Berkeley DROID Dataset** for Robotic Manipulation
- Trained Leaky-Integrate-and-Fire (LIF) neuron weights in **PyTorch**, performed **quantization** for hardware compatibility, and mapped parameters to fixed-point representations
- Designed LIF neuron modules using shift-register counters to emulate membrane potential dynamics and developed inter-layer **FIFO queues** to stage **asynchronous spike traffic**
- Streamed multi-gigabyte testing data through the **UART protocol** to the **FPGA** and back, testing inference accuracy against PyTorch model

32-bit Operating System January 2024 – May 2024
Systems Project C, x86, QEMU

- Programmed a 32-bit Operating System with a **3-terminal interface** for **IA-32** architecture using **x86 assembly and C**
- Developed a 2-Radix **Paging System** and **Allocator** for both 4KB and 4MB page
- Constructed a simple **virtual file-system** and over 10 **system call handlers** to interface with the kernel and the physical file-system
- Designed a **Round Robin Scheduling algorithm** for switching between various userspace programs

Convolutional Neural Network Optimization January 2024 – May 2024
Parallel Algorithm and Profiling Project CUDA, C++

- Researched and implemented a scalable **CNN forward pass layer** using **CUDA**, and verified optimization efficiency through the use of Nvidia Nsight Systems and Compute
- Optimized convolutions through the use of streams, **shared memory**, constant memory, matrix unrolling, **tensor cores**, and using custom **half2** data types

Student Organizations

Engineering Tutor January 2024–Present
Eta Kappa Nu Honor Society Champaign, IL

- Inducted as a **top 20% student** in the department; tutor peers in topics ranging from LC-3 **assembly** and **C** programming to analog **signal processing**, **multivariable calculus**, and **architecture design**
- Create custom study guides and **host review sessions** across 5+ engineering courses, supporting **100+ students** in exam preparation

SIGArch Champaign, IL
Member January 2023 – Present

- Facilitated **technical discussions and reading groups** on computer architecture topics, including modern **CPUs**, **GPUs**, and **emerging accelerator designs**
- Helped coordinate architecture-focused talks and workshops featuring graduate students and faculty working on **microarchitecture, memory systems, and parallel computing**
- Collaborated with other **computing organizations** to host events bridging architecture with **systems, compilers, and hardware-software co-design**
- Supported **professional and academic networking events** connecting undergraduate students with graduate researchers and industry professionals in computer architecture

Social Chair May 2023 – May 2024
Association for Computing Machinery Champaign, IL

- Organized and hosted **50+ social events**, including weekly social hours that connected engineering students from freshmen to graduate levels
- **Expanded organization membership** by over 300 students through active community engagement and **cross-disciplinary outreach**
- Collaborated with **4+ campus organizations** to **plan minority-inclusive events** and co-host a large-scale joint school dance
- Assisted in coordinating **12+ professional networking events**, enabling students to engage with **industry professionals** across diverse computing disciplines